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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,169	04/09/2001	Stephen C. Vincent	P04860US0	8267

22885 7590 05/13/2003

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EXAMINER	
MCDONALD, RODNEY GLENN	

16

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 05/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/829,169	Applicant(s) Vincent
	Examiner Rodney McDonald	Art Unit 1753

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If the period for reply specified above is the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Mar 5, 2003*

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-5 and 15* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-5 and 15* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 16
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 and 3-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Copetti et al. (U.S. Pat. Pub. 2001/0017770).

(It should be noted that this rejection is made giving weight to the limitation of newly added claim limitation "chip" although the Examiner believes that the previous rejections made in the Office Action of 11-27-02 are still applicable and are also included in this Office Action to teach production of the layered structure)

Copetti et al. teach that their invention relates to a module for electronic device usable in TV sets and video recorder. (This indicates utilizing the layered material as chip usage) (Page 1 paragraph [0001, 0002, 0003])

In Fig. 1 the module with a thin-film circuit has ***a substrate 1*** which comprises a ceramic material, a glass-ceramic material, a glass material or a ceramic material. ***A barrier layer 8 may be provided on the substrate 1. A resistance layer 7 is deposited on the substrate 1 or the barrier layer 8. This structured resistance layer 7 may comprise*** $Ni_xCr_yAl_z$ ***($0 \leq x \leq 1$; $0 \leq y \leq 1$; $0 \leq z \leq 1$).*** A first electrically conductive layer 2 is provided on this resistance layer 7 and is structured. ***A dielectric 3 is present on this structured first electrically conducting layer L, which dielectric 3 will normally cover the entire surface area of the substrate 1*** and is interrupted in certain locations only so as to create vias to the subadjacent first structure electrically conducting layer 2. ***The dielectric 3 may comprise*** Ta_2O_5. The first electrically conducting layer 2 may comprise Cu, Al, Al doped with a few percents of Cu, Al doped with a few percents of Si, Al doped with a few percents of Mg, or Al doped with a few percents of Cu and Si. (Page 2 paragraph [0060]; Page 3 paragraph [0060])

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minami et al. (U.S. Pat. 4,777,583).

Figure 2 is representative of the invention. In Fig. 2 numerals 1, 2, 3, 4, 5, 6 represent a ceramic substrate, a glaze layer, ***a heat-generating resistor***, a common electrode, an individual electrode and a protecting film, respectively. (Column 3 lines 55-60) A known alumina ceramic is used as the ceramic substrate. (Column 3 lines 60-61) The glaze layer 2 is partially formed on the ceramic substrate 1. (Column 4 lines 5-6) The ***heat-generating resistors 3*** and ***electrodes 4 and 5*** are formed to have shapes shown in Fig. 1. A number of independent rows of heat-generating resistors 3 are formed on the glaze layer 2 at small intervals t in the longitudinal direction, and electrodes 4 and 5 having a width W are formed on the glaze layer 2 at small intervals t in the longitudinal direction. (Column 4 lines 25-31) ***Titanium***, chromium silicate, tantalum silicate, and tantalum nitride may be used ***as the heat-generating resistor 3*** and it is generally preferred that the thickness of the heat-generating resistors 3 be 0.05 to 0.5 microns. Aluminum or gold is used as the material constituting the ***electrodes 4 and 5***, and it is preferred that the thickness of the electrodes 4 and 5 be 0.5 to 2.0 microns. (Column 4 lines 63-68; Column 5 lines 1-2) A ***protecting film 6*** may be formed on the heat generating resistors 3 and the electrodes 4 and 5, as shown in Fig. 2. A material excellent in the oxygen barrier property, the thermal conductivity, the electrically insulating property and the abrasion resistance, such as ***tantalum pentoxide***, is used

for protecting film 6, and the thickness of the protecting film 6 is ordinarily 1.0 to 8.0 microns. (Column 5 lines 45-52)

The differences between Minami et al. and the present claims is the depositing of the layers is not discussed, where electrodes 4a and 5a are terminations is not discussed and the reduction of failures due to electrolytic corrosion under powered moisture conditions is not discussed.

As to the depositing the layers are deposited in order to achieve the structure of Figure 2 and must be deposited in that order such that the layers overlay one another. (See Figure 2)

As to the terminations since 4a and 5a are electrodes they are the terminations of the structure which are on the ends of the metal film as seen in Figs. 1 and 2. (See Figures 1 and 2)

As to the reduction of failures due to electrolytic corrosion under powered moisture conditions, it is believed that since tantalum pentoxide serves as a protective film it will protect the layers form moisture and corrosion. (See Column 5 lines 45-52)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed a thin film resistor with moisture barrier layer as taught by Minami et al. because it allows for utilizing resistors to form thermal heads.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minami et al. (U.S. Pat. 4,777,583) as applied to claim 1 above, and further in view of Young (U.S. Pat. 4,002,542).

The differences not yet discussed is the depositing by sputtering of the tantalum pentoxide layer.

Young teach in Fig. 1 a dielectric substrate 10 to which is applied a non-tantalum electrically conductive film electrode 12. The material of the dielectric substrate 10 may be any suitable dielectric material such as glass, ceramic, glass-ceramics or the like. The material of the electrode 12 may be any electrically conductive material which is compatible with tantalum oxide as well as compatible with the method of applying a film of tantalum oxide thereto, such as for example as aluminum, chromium nichrome, or the like. (Column 2 lines 20-30)

The dielectric substrate-electrode composite of FIG. 1 is disposed on substrate holder 16 while a target of tantalum oxide 22 is disposed on target holder 20 within housing 18. Housing 18 is then sealed and a predetermined desired vacuum is drawn therein. The amount of vacuum drawn depends on the materials involved in the sputtering as well as, to some extent, on the electrical parameters of the various parts of the apparatus. A quantity of inert ionizable gas is then introduced into housing 18 reducing the vacuum to a predetermined desired level. One familiar with the art can readily select a suitable level of vacuum for a specific set of parameters. The ionizable gas may be any suitable inert ionizable gas such as argon, xenon, nitrogen, or the like. A plasma is then initiated by means of filament cathode 24, anode 26, and dc power sources 36 and 37, while suitable r-f energy is applied to target material 22 by r-f power source 38. If desired, magnetic coils 40 and 42 may be energized to focus the plasma. Under these described conditions, ***target material 22 will be caused to sputter*** and be applied over electrode 12 on substrate 10. When desired, a mask may be interposed over electrode 12 to pattern the application of the target material on electrode 12. Such a mask is not shown, however, its nature will be readily

understood by one familiar with the art. ***After a suitable sputtering period of time, a layer or film 44 of target material 22 will be applied to electrode 12 as illustrated in FIG. 3. As heretofore described, the target material for thin film capacitors will be tantalum oxide, Ta2O5,*** which will comprise the capacitor dielectric. ***Although the proceeding describes a process of r-f triode sputtering from a Ta2O5 target, layer or film 44 may be applied by reactive sputtering from a tantalum target, by electron beam evaporation from a Ta2O5 target, by r-f diode sputtering from a Ta2O5 target, or by like methods.*** (Column 2 lines 57-68; Column 3 lines 1-24)

The motivation for depositing the tantalum pentoxide layer through sputtering is that it allows for depositing a film without reduced electrical series resistance. (Column 1 lines 32-35)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Minami et al. by sputter depositing the tantalum pentoxide film as taught by Young because it allows for depositing a film without reduced electrical series resistance.

6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minami et al. as applied to claim 1 above, and further in view of Oki Electric Ind Co Ltd (Japan 52-3196).

The differences not yet discussed is the resistance layer being NiCr.

Minami et al. recognize that resistance layers to be used can be Ti and tantalum nitride, etc. (See Minami et al.)

Oki Electric Co. Ltd. Also recognize that resistance layers can be tantalum nitride, NiCr, etc. (See Oki Electric Co. Ltd. Abstract)

The motivation for replacing Minami et al.'s resistive layer with NiCr of Oki is that it allows for providing a layer with the required resistance feature. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art to have modified Minami et al. by replacing their resistive layer with a layer of NiCr as taught by Oki Electric Co. Ltd. because the resistive layers are art recognized equivalents.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over in Fuyama et al. (U.S. Pat. 4,617,575) view of Sato (Japan 61-27264) and Oki Electric Ind Co Ltd (Japan 52-3196).

Fuyama et al. teach in Fig. 1 ***a heating resistor 110*** of chromium silicon alloy having a thickness of 0.1 microns and first layer conductor 120 consisting of a chromium layer 10 and an aluminum layer 20 are formed in a predetermined pattern on an alumina substrate 100 with a glaze layer as an insulating substrate. Then, a protective film 140 made of silicon dioxide and serving as an insulating film at the same time is formed thereon throughout the entire surface by ***sputtering*** or plasma CVD so far used, preferably, to a thickness of about 3 microns. Then, a silicon nitride film 150 is formed only on the heating resistor 110 by mask plasma CVD. Crack formation can be prevented by the release of the stress on the silicon nitride. (Column 4 lines 19-35) ***Tantalum pentoxide*** can be used alternatively to the silicon nitride. (Column 3 lines 30-33)

The differences between Fuyama et al. and the present claims is that depositing the films is not discussed, the resistive film being a metal film is not discussed and the reduction of failures due to electrolytic corrosion under powered moisture conditions is not discussed.

Sato teach in preparing a thermal head, ***an abrasion resistant layer 6 being a protective layer comprising tantalum pentoxide*** is formed in a thickness of about 5 microns by a sputtering method and heat-treated in air or a nitrogen atmosphere. This heat treatment is performed at a temperature equal to or higher than a peak temperature generated by the pulse driving or a heat generating resistor 2 to make it possible to impart a good characteristic for reducing the change ratio in the resistance value of the heat generating resistor 3. The relation of the resistance change ratio of thus formed thermal head and a pulse number is reduced in variation and stabilized over a long period of time and, because a heat treatment process is performed ***after each layer was formed by a sputtering method***, there is no interruption in the process and manufacturing cost can be reduced. (See Abstract)

The motivation for depositing each layer by a sputtering method is that it allows for no interruption in the manufacturing cost. (See Abstract)

Oki Electric Co. Ltd. teach that ***resistance layers can be metals such as W, NiCr***, etc. (See Oki Electric Co. Ltd. Abstract)

The motivation for utilizing resistance layers of metal is that it allows for providing a layer with the required resistance feature. (See Abstract)

As to the reduction of failures due to electrolytic corrosion under powered moisture conditions, since the tantalum pentoxide can be used as a protective layer it would protect against electrolytic corrosion. (See Fuyama et al. Column 3 lines 30-33)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Fuyama et al. by depositing the layers by sputtering as taught by Sato and to have utilized metals as the resistance layers as taught by Oki Electric Co. Ltd. because it allows for no interruption in the manufacturing cost and for providing a layer with the required resistance feature.

8. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Copetti et al. (U.S. Pat. Pub. 2001/0017770) in view of Young et al. (U.S. Pat. 4,002,542).

(It should be noted that this rejection is made giving weight to the limitation of newly added claim limitation "chip" although the Examiner believes that the previous rejections made in the Office Action of 11-27-02 are still applicable and are also included in this Office Action to teach production of the layered structure)

Copetti et al. is discussed above and all is as applies above. (See Copetti et al. discussed above)

The differences between Copetti et al. and the present claims is that depositing Ta_2O_5 by sputtering is not discussed.

Young is discussed above and teach sputtering a layer of tantalum pentaoxide. (See Young discussed above)

The motivation for depositing the tantalum pentoxide layer through sputtering is that it allows for depositing a film without reduced electrical series resistance. (Column 1 lines 32-35)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Copetti et al. by sputtering a layer of tantalum pentaoxide as taught by Young et al. because it allows for depositing a film without reduced electrical series resistance.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Copetti et al. (U.S. Pat. Pub. 2001/0017770) in view of Fuyama et al. (U.S. Pat. 4,617,575).

(It should be noted that this rejection is made giving weight to the limitation of newly added claim limitation "chip" although the Examiner believes that the previous rejections made in the Office Action of 11-27-02 are still applicable and are also included in this Office Action to teach production of the layered structure)

Copetti et al. is discussed above and all is as applies above. (See Copetti et al. discussed above)

The differences between Copetti et al. and the present claims is that depositing a layer of passivation on the substrate is not discussed.

Fuyama et al. is discussed above and teach utilizing a passivation layer of silicon dioxide under the a film of tantalum pentaoxide. (See Fuyama et al. discussed above)

The motivation for utilizing a layer of passivation under the film of tantalum pentaoxide is that it allows for serving as a protective and insulating film. (Column 4 lines 19-35)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Copetti et al. by utilizing a passivation film as taught by Fuyama et al. because it allows for serving as a protective and insulating film.

Response to Arguments

10. Applicant's arguments filed March 5, 2003 have been fully considered but they are not persuasive.

RESPONSE TO THE ARGUMENTS:

In response to the argument that the references do not teach the same layers in the same relationship as required by the claims (i.e. directly overlying and attaching the substrate), it is argued that Minami et al. do teach the same layers in the same relationship as required by Applicant's claims. The layers do overlie the substrate. The layers do attach directly to the substrate on either side of layer 2 thus reading on Applicant's claims. (See Minami et al. discussed above)

In response to the argument that the references do not teach a chip resistor, it is argued that the Minami suggest the method of forming the required layers of Applicant's claims. No weight for the product limitation (i.e. chip) is given utilizing this consideration. However if weight is given to this product limitation (i.e. chip) it is believed that Copetti et al. teach the "chip" limitation or at least suggest the "chip" limitation since their substrate is utilized in electronic devices. Furthermore Copetti et al. teach the making the required layer structure. (See Minami et al. and Copetti et al. discussed above)

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney McDonald whose telephone number is 703-308-3807. The examiner can normally be reached on M-Th from 8 to 5:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen, can be reached on (703) 308-3322. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9310.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

RODNEY G. MCDONALD
PRIMARY EXAMINER

RM

May 9, 2003